



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,666	01/22/2004	Carlos Dangelo	NANOC002NP	5164
24341	7590	05/09/2005	EXAMINER	
MORGAN, LEWIS & BOCKIUS, LLP. 2 PALO ALTO SQUARE 3000 EL CAMINO REAL PALO ALTO, CA 94306			PAREKH, NITIN	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

\$/EX

Office Action Summary	Application No.	Applicant(s)	
	10/762,666	DANGELO, CARLOS	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) 1-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 22-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>01-22-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION***Election/Restriction***

1. Applicant's election with traverse of Group I, claims 22-32 in Paper No. 3 is acknowledged. The traversal is on the ground(s) that in the requirement for an election, Groups I and II differ only in a semiconductor device and method for making the same. Requiring an election based on the above-noted differences would appear to be unwarrant since the fields of search appear to be almost identical. This is not found persuasive because referring to the restriction requirement set forth in the Office Action paper no.2, it clearly shows that the alternative method proposed by the examiner would be distinct from the process claimed. Additionally, the search is not coextensive as evidenced by the different fields of search for the process and product as cited in the previous restriction requirement. Furthermore, Applicant has not provided a convincing argument that the materially different processes would not be suitable in producing the claimed device.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 22-26 are rejected under 35 U.S.C. 102(a) as being anticipated by Awano (US Pat. Application Pub. 2002/0163079).

Regarding claim 22 and 23, Awano discloses an integrated circuit structure/device (ICS- see Fig. 4) comprising a heat conducting structure/device (see 37 in Fig. 4; see 0072 and 0085), the ICS comprising:

- a plurality of vias/carbon nanotubes comprising those connecting a plurality of wiring lines/interconnect levels (see 36 connecting 35 at different levels in Fig. 4) and those comprising a heat conductive network of a plurality of contact structures/heat conductive vias/carbon nanotubes (see 37 through 33a-33f in Fig. 4) extending from a top surface of an active device layer (32 in Fig. 4), through a plurality of wiring lines/interconnect levels (see 35 in Fig. 4), to a top surface of the ICS
- the heat conductive vias traversing the interconnect levels, and
- the heat generated by active devices in the device layer being conducted through the heat conductive network of contact structures/heat conductive vias/carbon nanotubes to the top surface of the ICS

(Fig. 4 ; sections 0087 and 0071-0086).

Awano further discloses the contact structures/heat conductive vias/carbon nanotubes being electrically isolated from metal/via conductors of wiring lines/interconnect levels

(see 37 and 36 in Fig. 4) and a portion of wiring members/metal conductors and the wiring lines/interconnect levels being formed of a metal other than carbon nanotubes (section 0086).

Regarding claim 24, Amano discloses the entire claimed structure as applied to claim 22 above, wherein Amano teaches the wiring/via structure comprising conventional material such as copper or aluminum (section 0008).

Regarding claim 25, Amano discloses the entire claimed structure as applied to claim 22 above, wherein Amano teaches the plurality of contact structures/heat conductive vias/carbon nanotubes being oriented in a direct line from the top surface of the active device layer to that of the ICS (see 37 in Fig. 4).

Regarding claim 26, Amano discloses the entire claimed structure as applied to claim 22 above, wherein Amano teaches each via in the plurality of contact structures/heat conductive vias/carbon nanotubes (see 16 in Fig. 1) traversing a single level of wiring line/interconnect (see 14 in Fig. 1) wherein the single level of wiring line/interconnect comprises a single layer of interconnect metal over a single layer of intermetal dielectric (see 13 in Fig. 1; section 0075).

4. Claims 27-32 are rejected under 35 U.S.C. 102(a) as being anticipated by Dahl et al. (US Pat. Application Pub. 2002/0130407).

Regarding claims 27, 29 and 30, Dahl et al. disclose an integrated circuit (IC) chip substrate/die having enhanced power dissipation and improved heat transfer structure (see 601 in Fig. 6C), the IC chip/die comprising:

- a substrate having a top surface upon which power generating devices of the IC are fabricated (see sections 0116 and 0136; Fig. 6 and 9) and a back/bottom surface essentially parallel to the top surface
- a plurality of cavities/holes (see 633/634 in Fig. 6C) extending a predetermined distance from the bottom surface to the top surface, the predetermined distance being less than the distance between the top and bottom surfaces, the cavities/holes being filled with heat conductive media (HCM) in a form of conducting conduits/thermal vias including highly thermally conductive material comprising a variety of diamond containing material, carbon nanotubes, etc. (sections 0007 and 0118-0122) and the cavities/holes being distributed/located directly below the IC devices/power generating devices of the substrate to provide the heat removal from the desired areas of the substrate (see Fig. 6C)

Art Unit: 2811

- the HCM having thermal conductivity greater than that of conventional heat spreading/thermally conductive metal such as copper or the silicon substrate, and
- the heat produced by the IC devices/power generating devices being transferred to the back/bottom surface via the HCM

(Fig. 6C; sections 00116-0122).

Regarding claim 28, Dahl et al. disclose the entire claimed structure as applied to claim 27 above, wherein Dahl et al. teach using conventional heat spreading material such as copper or aluminum (section 0118).

Regarding claims 31 and 32, Dahl et al. disclose the entire claimed structure as applied to claim 27 above, wherein Dahl et al. teach the IC devices/power generating devices comprising transistors having source/drain regions (see 902 in Fig. 9; section 0136) , such device configuration in the IC package having the plurality of cavities/HCM being distributed/located along the bottom surface of the substrate (see Fig. 6C) provides the cavities/HCM directly below respective source, drain and isolation regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

Art Unit: 2811

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

04-18-05



NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800